CLAIMS

1. An apparatus for use in performing a floating point multiply-accumulate operation, comprising:

a plurality of latches that contain a plurality of exponents of operands for the operation;

a carry-save adder, coupled to the latches, that receives the exponents of operands and performs a carry-save add operation on the exponents of operands to produce a first result; and

a logic block, coupled to the carry-save adder, that receives the first result and performs a carry-lookahead add operation on the first result to produce a second result, the logic block having a logic circuit that performs an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation.

2. The apparatus of claim 1, wherein the logic circuit includes a redundant logic stage for processing said most significant bit in the logic block.

3. The apparatus of claim 2, wherein the redundant logic stage performs the logic operation on the most significant bit in parallel with at least a portion of the carry-lookahead add operation.

4. The apparatus of claim 1, wherein the logic circuit performs the logic operation to produce a shift value for use in the floating point multiply-accumulate operation.

5. The apparatus of claim 1, further including a control circuit for generating the control signal.

6. The apparatus of claim 5, wherein the control circuit generates the control signal based upon a Single Instruction Multiple Data operation.

7. The apparatus of claim 5, wherein the control signal is a pair of complementary signals and wherein the control circuit generates the pair of complementary signals.

8. The apparatus of claim 1, wherein the logic block includes a carry-lookahead adder having complementary logic circuits for providing complementary outputs as the second result.

9. A method for use in performing a floating point multiply-accumulate operation, comprising:

receiving a plurality of exponents of operands for the operation;

performing a carry-save add operation on the exponents of operands to produce a first result;

performing a carry-lookahead add operation on the first result to produce a second result;

receiving a control signal; and

performing an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation.

10. The method of claim 9, wherein the performing the logic operation step includes using a redundant logic stage for processing said most significant bit in a carry-lookahead adder circuit.

11. The method of claim 10, wherein the using step includes processing the most significant bit in parallel with at least a portion of the step of performing the carry-lookahead add operation.

12. The method of claim 9, wherein the performing the logic operation step includes producing a shift value for use in the floating point multiply-accumulate operation.

13. The method of claim 9, further including generating the control signal.

14. The method of claim 13, wherein the generating step includes generating the control signal based upon a Single Instruction Multiple Data operation.

15. The method of claim 13, wherein the generating step includes generating a pair of complementary signals as the control signal.

16. The method of claim 9, wherein the performing the carry-lookahead add operation step includes using complementary logic circuits for the carry-lookahead add operation to provide complementary outputs as the second result.